LISTING OF CLAIMS

This listing of claims replaces all prior versions and listings of claims in the application:

Claims

1. (Currently Amended) A computer system including:

a processor;

a first controller;

a random access memory having a plurality of locations for volatile storage of data; and

a data communications facility interconnecting said processor, said first controller, and said random access memory;

wherein said first controller is responsive to a command received from the processor to commence transmission of a quantity of data from a first random access memory location to a second random access memory location, wherein said ~~single~~ command specifies said first and second random access memory locations, with the first controller monitoring operation of the processor to terminate the transmission of the data to the second random access memory location, ~~before~~ during transmission of the quantity ~~has been transmitted~~ thereto, in response to the processor generating a write request to the second random memory location.

2. (Previously Presented) The system of claim 1, wherein said random access memory is coupled to said data communications facility via a memory controller, said memory controller configured manage operations for said random access memory.

3. (Previously Presented) The system of claim 2, wherein the data is copied from the first random access memory location to the second random access memory location by an internal memory transfer, without traveling over the data communications facility.

4. (Previously Presented) The system of claim 2, wherein said first controller is provided by said memory controller.

5. (Currently Amended) The system of claim 1, wherein a first portion of the random access memory is coupled to said data communications facility via a first memory controller and includes said first random access memory location, and a second portion of random access memory is coupled to said data communications facility via a second memory controller and includes said second random access memory location.

6. (Previously Presented) The system of claim 5, wherein data is copied from the first random access memory location to the second random access memory location by using a peer-to-peer copy operation on the data communication facility.

7. (Original) The system of claim 6, wherein said data communications facility supports direct memory access (DMA), and said peer-to-peer copy operation is performed by using a transaction analogous to DMA.

8. (Previously Presented) The system of claim 5, wherein said first controller is provided by said first and second memory controllers.

9. (Previously Presented) The system of claim 1, wherein the first controller maintains a record of copy operations that are in progress.

10. (Previously Presented) The system of claim 1, wherein the processor continues processing operations prior to data being completely copied to the second random access memory location .

11. (Previously Presented) The system of claim 10, wherein the first controller redirects a read request for the second random access memory location to the first random access memory location if the copy has not yet completed.

12. (Previously Presented) The system of claim 10, wherein the first controller delays a write request for the first random access memory location pending completion of the copy.

13. (Canceled)

14. (Previously Presented) The system of claim 1, further comprising a cache, and wherein any cache entry for the second random access memory location is invalidated in response to said command.

15. (Previously Presented) The system of claim 14, wherein any cache entry for the second random access memory location is invalidated by the processor.

16. (Previously Presented) The system of claim 14, wherein any updated cache entry for the first memory random access location is flushed to memory in response to said command.

17. (Previously Presented) The system of claim 1, wherein said processor supports a specific programming command to copy data from a first random access memory location to a second random access memory location.

18. (Original) The system of claim 1, wherein said data communications facility is a bus.

19. (Previously Presented) The system of claim 18, wherein said bus supports a command set, and said command is part of said command set.

20. (Previously Presented) The system of claim 1, wherein said first controller transmits an acknowledgement of said command back to the processor, and wherein the processor is responsive to a failure to receive said acknowledgement within a predetermined time-out period to perform said copy operation by issuing separate read and write commands.

21. (Canceled)

22. (Currently Amended) A method for operating a computer system including a processor, a first controller, a random access memory having a plurality of locations for

volatile storage of data, and a data communications facility interconnecting said processor, said first controller, and said random access memory, said method comprising:

issuing a command from the processor to the first controller, said command specifying a first random access memory location and a second random access memory location; and

responsive to receipt of said command by the first controller, commencing transmission of a quantity of data from the first random access memory location to the second random access memory location; and

terminating the transmission of the data to the second random access memory location, ~~before~~ during transmission of the quantity ~~has been transmitted~~ thereto, in response to the processor generating a write request to the second random memory location.

23. (Previously Presented) The method of claim 22, wherein said data communications facility is a bus that supports a command set, and said command is part of said command set.

24. (Previously Presented) The method of claim 22, wherein the data is copied from the first random access memory location to the second random access memory location by an internal memory transfer, without traveling over the data communications facility.

25. (Previously Presented) The method of claim 22, wherein the processor continues processing operations prior to data being completely copied to the second random access memory location .

26. (Previously Presented) The method of claim 25, further comprising redirecting a read request for the second random access memory location to the first random access memory location if the copy has not yet completed.

27. (Previously Presented) The method of claim 25, further comprising delaying a write request for the first random access memory location pending completion of the copy.

28. (Canceled)

29. (Previously Presented) The method of claim 22, wherein the computer system further comprises a cache, and wherein said method further comprises invalidating any cache entry for the second random access memory location in response to said command.

30. (Previously Presented) The method of claim 29, further comprising flushing any updated cache entry for the first random access memory location to random access memory in response to said command.